UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,063	08/05/2003	Giulio Casagrande	856063.660D1	1308

500 7590 03/24/2005

SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVE
SUITE 6300
SEATTLE, WA 98104-7092

EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/635,063	CASAGRANDE ET AL.	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Remarks filed on December 7, 2004.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-3 are rejected under 35 U.S.C. 102(a) as being anticipated by Nakamura et al. (US 5,986,299).

In re claim 1, Nakamura et al. discloses (col. 2, line 49 - 63 and col. 8, line 57-col. 13, line 45 and figs. 3-5) a method of fabricating a memory cell integrated in a semiconductor substrate comprising: forming, on the semiconductor substrate (1), a MOS transistor having first and second conduction terminals (3 and 4), forming a first protective layers (8) over the MOS transistor, forming and patterning one or more metallization layers (11) over the MOS transistor, forming a second protective layer (18) over the one or more metallization layers (11) and forming a capacitive element (20, 21, 22) coupled in series with the MOS device, including defining a lower electrode (20) of the capacitive element on the second protective layer. The capacitive element is formed after all of the one or more metallization layers are formed and patterned without forming and patterning any additional metallization layer after the capacitive element is formed (col. 12, line 55 – col. 12, line 30).

In re claim 2, Nakamura discloses (fig. 3) the method further comprising: forming a plurality of contact vias (10, 13, 16, 19) through the first and second protective layers for establishing an electrical connection between the lower electrode (20) of the capacitive element and at least one of the conduction terminals (3) of the MOS device.

In re claim 3, Nakamura discloses (col. 13, lines 30-45) the method wherein forming a capacitive element comprises forming a ferroelectric capacitor having a ferroelectric material layer for a dielectric layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. (US 5,986,299) as applied to claim 1 above, and further in view of Leung et al. (US 5,563,762).

In re claim 4, Nakamura discloses (fig. 3) the method wherein the one or more metallization layers includes a first metallization layer (11) formed on the first protective layer and a second metallization layer (14) formed between the second protective layer (18) and a third protective layer (15) positioned between the first and second protective layers. Nakamura does not disclose the method further comprising forming a pad area from the second metallization layer and electrically connecting the pad area to an upper

electrode of the capacitive element. Leung shows (figs. 5-10) the method of forming a forming a pad area (106) from the second metallization layer and electrically connecting the pad area to an upper electrode (134) of the capacitive element. With this method, very large capacitors can be provided on top of the integrated circuit without limiting the interconnect routing efficiency of the underlying integrated circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the connection scheme of Nakamura by forming a pad connected to the first metallization as taught by Leung to provide very large capacitors without limiting the interconnect routing efficiency of the underlying integrated circuit.

In re claim 5, Leung discloses (fig. 3) the method further comprising forming a flat (126) on the second protective layer and electrically coupling the flat to the upper electrode (134) of the capacitive element, and forming an electrical contact (124) that extends through the second protective layer between the pad area to the flat.

In re claim 6, Nakamura discloses (figs. 3-5) the one or more metallization layers includes a first metallization layer (11) formed on the first protective layer and a second metallization layer (17) formed between the second protective layer (19) and a third protective layer (15) positioned between the first and second protective layers. Leung shows (figs. 5-10) the method of forming a pad area (104) from the second metallization layer before forming the second protective layer (114, 116); and removing a portion of the second protective layer from the pad area after the capacitive element is formed, thereby exposing the pad area for an external connection (col. 9, lines 57-63).

In re claim 7, Nakamura discloses (figs. 3-5) the one or more metallization layers includes a first metallization layer (11) formed on the first protective layer and a second metallization layer (17) formed between the second protective layer and a third protective layer positioned between the first and second protective layers. Leung shows (figs. 5-10) the method further comprising forming a third metallization layer (124) on the second protective layer before forming the lower electrode (128) on the second protective layer.

Claims 8-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. (US 5,986,299) in view of Leung et al. (US 5,563,762).

In re claim 8, Nakamura et al. discloses (col. 2, line 49 - 63 and col. 8, line 57-col. 13, line 45 and figs. 3-5) a method of making a memory cell integrated in a semiconductor substrate, the method comprising: forming a MOS transistor (3, 4); forming a plurality of metallization layers (11, 14, 17) including a first metallization layer (11), the plurality of metallization layers overlaying the MOS device; covering the first metallization layer with a top insulating layer (18); forming a capacitive element (20, 21, 22) on the top insulating layer after forming the plurality of metallization layers, the capacitive element having a lower electrode (20) covered with a layer of a dielectric material (21) and capacitively coupled to an upper electrode (224). Nakamura shows all of the elements of the claims except the method of forming a flat on the top insulating layer; electrically connecting the flat to the upper electrode by a plate line; and electrically connecting the flat to a pad of the first metallization layer. Leung shows

(figs. 5-10) the method of forming a flat (126) on the top insulating layer; electrically connecting the flat to the upper electrode by a plate line (134); and electrically connecting the flat to a pad (106) of the first metallization layer such that the memory cell may be driven through the pad of the first metallization layer provided beneath the capacitive element. With this method, very large capacitors can be provided on top of the integrated circuit without limiting the interconnect routing efficiency of the underlying integrated circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the connection schemer of Nakamura by forming a flat connected to the first metallization as taught by Leung to provide very large capacitors without limiting the interconnect routing efficiency of the underlying integrated circuit.

In re claim 9, Leung discloses (col. 9, lines 22-29 and fig. 8) that the flat (126) and the lower electrode (128) are formed by forming a conductive layer on the top insulating layer and defining the flat and the lower electrode from the conductive layer.

In re claim 10, Nakamura et al. discloses (figs. 3-5) the method further comprising: forming a bottom insulating layer (8) on the substrate; and forming a plurality of contact vias (10, 13, 19) through the bottom and top insulating layers for establishing an electrical connection between the lower electrode of the capacitive element and a conduction terminal of the MOS transistor.

In re claim 11, Leung discloses (figs. 5-8) the method wherein electrically connecting the flat to the first metallization layer includes forming a pad area (106) from

the first metallization layer; and forming a contact (124) that extends through the top insulating layer and electrically connects the pad area to the flat.

In re claim 12, Leung discloses (col. 9, lines 1-64 and fig. 3) the method wherein the pad area (104) is formed before forming the top insulating layer (114, 116), the method further comprising removing a portion of the top protective layer from the pad area after the capacitive element is formed, thereby exposing the pad area for an external connection (col. 9, lines 57-63).

In re claim 13, Leung discloses (col. 9, lines 1-64 and fig. 3) the method further comprising forming a second metallization layer on the top protective layer and defining the second metallization layer into a first pad area before forming the lower electrode on the top insulating layer, and connecting the first pad area to a second pad area formed from the first metallization layer.

In re claim 14, Nakamura et al. (US 5,986,299) a method of forming a memory device integrated in a semiconductor substrate, the method comprising; forming a matrix of memory cells (array of cells col. 5, lines 9-24) each including a MOS device (3,4) and a capacitive element (20, 21, 22), the matrix being formed by: forming a plurality of metallization layers (11, 14, 17) including a top metallization layer (17), the plurality of metallization layers being formed between the MOS devices and the capacitive elements of the memory cells; covering the top metallization layer with a top insulating layer (18); forming the capacitive elements on the top insulating layer after forming the plurality of metallization layers, each capacitive element having a lower

electrode (20) covered with a layer of a dielectric material (21) and capacitively coupled to an upper electrode (22); Nakamura shows all of the elements of the claims except the method of forming a flat on the top insulating layer; electrically connecting the flat to the upper electrode by a plate line; and electrically connecting the flat to a pad of the first metallization layer. Leung shows (figs. 5-10) the method of forming a conductive flat (126) on the top insulating layer and outside of the memory matrix; and electrically connecting the flat to the upper electrodes of a plurality of the capacitive elements through a plate line (part of 134) that forms and connects the upper electrodes of the plurality of capacitive elements. With this method, very large capacitors can be provided on top of the integrated circuit without limiting the interconnect routing efficiency of the underlying integrated circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the connection schemer of Nakamura by forming a flat connected to the first metallization as taught by Leung to provide very large capacitors without limiting the interconnect routing efficiency of the underlying integrated circuit.

In re claim 15, Leung discloses (fig. 3) the method further comprising electrically connecting the flat to a pad (106) of the first metallization layer such that the plurality of capacitive elements may be driven through the pad of the first metallization layer provided beneath the capacitive elements.

In re claim 16, Leung discloses (col. 9, lines 22-29 and fig. 8) the method wherein the flat and the lower electrodes of the capacitive elements are formed by forming a

conductive layer on the top insulating layer and defining the flat and the lower electrodes from the conductive layer.

In re claim 17, Nakamura discloses (fig. 3) the method wherein forming the matrix of memory cells includes; forming a bottom insulating layer (8) on the substrate; and forming a plurality of contact vias (10, 13, 16, 19) through the bottom and top insulating layers for establishing an electrical connection between the lower electrodes of the capacitive elements and conduction terminals of the MOS devices.

In re claim 18, Leung discloses (figs. 5-8) the method further comprising forming a pad area (106) from the first metallization layer; and forming a contact (124) that extends through the top insulating layer and electrically connects the pad area to the flat.

In re claim 19, Leung discloses (col. 9, lines 1-64 and fig. 3) the method wherein the pad area (104) is formed before forming the top insulating layer (114, 116), the method further comprising removing a portion of the top protective layer from the pad area after the capacitive element is formed, thereby exposing the pad area for an external connection (col. 9, lines 57-63).

In re claim 20, Leung discloses (col. 9, lines 1-64 and fig. 3) the method further comprising forming a second metallization layer on the top protective layer and defining the second metallization layer into a first pad area before forming the lower electrode on the top insulating layer, and connecting the first pad area to a second pad area formed from the first metallization layer.

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER

MEW
MEW
March 21, 2005